Regular Paper [Poster]

AUGUST 20, 2024 (DAY 1)

* Poster Set-up & Exhibition : August 20, 14:00 ~ 18:00
* Standing Time : August 20, 16:55 ~ 17:45

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Analog Circuits	5	A Hierarchical Tree-Structured Control Digital Low Drop-out Regulator with Status-Dumping Mechanism	PS-1
	26	A bandgap reference with low TC of 1.363ppm/℃ across wide temperature range for PMICs	PS-2
	28	An Ultra Low Temperature Coefficient Bandgap Voltage Reference with Fully MOS Mirror Mapping Circuitry	PS-3
	38	An All-Digital Standard-Cell-Based Resistive-Sensing Display Panel/Chip Crack Detector	PS-4
	54	A Fully Integrated Three Level Voltage Regulator with Fast Load Transient Response Using Current build-up mode in 28nm technology for SoC	PS-5
	60	3 Level Fully Integrated Voltage Regulator with Package Bond Wire Inductor for IoT Applications	PS-6
	71	Power-efficiency estimation of exponential horn driver circuit for low-power optical link	PS-7
	73	Phase Locked Loop with Ramp Generator for FMCW LiDAR TX in 28-nm CMOS	PS-8
	140	A DLL-Based Three-Step Time-to-Digital Converter for Time-of-Flight Applications	PS-9
	171	A Resilient All-Digital PLL Using Ping-Pong Delay Line	PS-10
	184	34.8 dB Gain, 7.7GHz Unity Gain Frequency, 4.2 mW Operational Transconductance Amplifier with Current Re-used Feed-Forward Technique	PS-11
	189	Low-Power Frequency-Mode Temperature Sensing Circuit with Subthreshold Operational Amplifier	PS-12
	211	A highly noise-immune TSP readout system with 2nd-order bandpass filtering current conveyor AFE	PS-13
	251	Reconfigurable Gaussian filtering TSP readout circuit for Flexible AMOLED Display	PS-14
Circuits and Systems for Emerging Technologies	16	Signal Shifting-based Reusable Redundant TSV Structure for Infrastructure TSV	PS-15
	104	3T1R Memristor Crossbar Architecture for Diverse Logic Implementation	PS-16
	107	An Efficient Error Correction Method for DMFBs with Node Redundancy Considering Node Levels	PS-17
	208	Calibrating the Dark Count Rate of Single Photon Avalanche Diodes Using Linear Regression	PS-18
	213	Optimized Stochastic Computing based Median Filter	PS-19
	247	Modeling of Chiplet-based 2.5D Packaging with Silicon Bridge	PS-20
Digital Circuits, Architecture, and Systems	7	22/16nm High Speed and Area Efficient Automotive Grade STT-MRAM Memory Compiler for 2~128Mb	PS-21
	8	Design of Digital Lock-in-Amplifier SoC for Gas Pipeline Inspection	PS-22
	11	A 28-nm 10.4-fJ/b Cryogenic embedded DRAM with 3T1C Gain Cell and MBIST at 4-Kelvin	PS-23
	22	Kyberator: A High-Efficiency FPGA-Based Multi-Mode CRYSTALS-Kyber Accelerator for Quantum-Resistant Security Applications	PS-24
	34	A Resource-Efficient Multi-core Multi-thread RISC-V-based System-on-Chip	PS-25
	53	A Delay Calibration Circuit for Time-Controlled Pre-Emphasis up to 3.8Gbps in Memory Interfaces	PS-26
	56	Fast-Lock ZQ Calibration Utilizing Charge Injection Technique for High Density Memory Systems	PS-27
	63	Effective Data-Width Aware ECC Scheme for HBM	PS-28
	65	Cost-Efficient Partially-Parallel LDPC Decoder Architecture for 50G-PON Standard	PS-29
	69	Evaluating the Impact of In-band ECC on GPU Performance	PS-30
	95	Improved Contrast Enhancement Algorithm for Night Vision Systems using Thermal Camera	PS-31
	96	Optimizing Transformer Hardware Acceleration: Advancing GELU Activation with Innovative Data Representation Techniques	PS-32
	105	Low-error Fixed-width Booth Multiplier with High-radix Booth Encoder	PS-33
	111	FPGA Design of a Masked AES Circuit with PPRM-based S-Box	PS-34
	116	Enhancing Efficiency in Computational Intensive Domains via Redundant Residue Number Systems	PS-35
	128	Design of a 3D-IC based AI-Vision SoC	PS-36
	155	Analysis and Design of CRC-based SENT Interface for Future Automotive Applications	PS-37
	159	An Approximate Multiplier Design Based on Mitchell's Algorithm	PS-38
	164	A Two-level Tracking Mechanism to Mitigate RowHammer Attacks	PS-39
	166	Integration of IP-Cores for the M3 Architecture with Low Area Overhead: Accelerator Support Module	PS-40
	187	PEMAC: A Posit EMAC with LDD & Logarithm Approximation	PS-41
	231	On-Device Eye Tracking System with Dual Lightweight AI Processors	PS-42
	237	The hardware implementation of QARMA-64 with RoCC on FPGA for memory encryption	PS-43
	242	System-on-Chip iot for Smart Poultry Manufacturing	PS-44
	245	Efficient Hardware Implementation of Nonlinear Activation Function For Inference Model	PS-45
	273	A Novel Area Efficient Approximate Stochastic Computing Approach for Edge Devices	PS-46

AUGUST 21, 2024 (DAY 2)

* Poster Set-up & Exhibition : August 21, 13:10 ~ 17:00
* Standing Time : August 21, 15:55 ~ 16:45

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	77	BS2: Bit-Serial Architecture Exploiting Weight Bit Sparsity for Efficient Deep Learning Acceleration	PS-48
	120	Resource-efficient DL Model Inference with Weight Clustering and Zero-skipping	PS-49
	121	Fast Performance and Power Profiler for SRAM Compute-in-Memory-based Accelerators	PS-50
	133	Simplified Real-time Categorized Vehicle Counting and Speed Estimation	PS-51
	135	Error-Resilient Binary Neural Network Inference with Selective Recompute-Based Error Correction	PS-52
	156	Hardware-aware Hierarchical Transformer using Softmax Low Probability Prediction	PS-53
	162	Integrating Noise Classification and Speech Enhancement Model for Hearing Aids	PS-54
	174	Integrating CNN and RCE Networks for Efficient On-Device Image Classification	PS-55
	194	A Hybrid Precision Network and Binary Processing Elements for 3D Hand Pose Estimation	PS-56
	220	Strategic Improvements in CNN Accelerators: Optimizing PE Utilization for MobileNetV2	PS-57
	236	Autoencoder-based Knowledge Distillation For Quantized YOLO Detector	PS-58
	243	Row-Efficient Pruning for In-Memory Convolutional Weight Mapping	PS-59
	244	An Im2col Architecture Using The Benes Network For Deep Learning Hardware Accelerators	PS-60
	250	C-AFA: A Conditionally Approximate Full Adder for Efficient DNN Inference in CIM Arrays	PS-61
	263	Generative Adversarial Network (GAN)-based Spiking Neural Network Training Methodology to Improve Computing Accuracy	PS-62
	269	Lightweight DL-based Drone Image Classification for Surveillance Applications	PS-63
	275	Tailoring Backbone Architectures for SSD	PS-64
RF/Microwave/Wireless	30	1×8 patch antenna array on glass/PCB substrate	PS-65
	125	A 60 GHz CMOS OOK Receiver with 7.7 GHz Bandwidth for Wireless Proximity Communication	PS-66
	142	A 5.8GHz Bootstrap Rectifier for Wireless RF Power Tranfer	PS-67
	143	Low-cost SDR-based Reader for Chipless Sensor Tag	PS-68
	198	Differential Injection-Locked Frequency Tripler with a Low-coupling 8-shaped Transformer	PS-69
SoC Design Methodology and CAD	14	LogicEdu: Enhancing Computational Logic Understanding through Web-Based Boolean Logic Simplification Tool	PS-70
	21	Scan Architecture with Data Observation for Multiple Scan Cell Fault Diagnosis	PS-71
	33	INC: In channel Crossing ECC for LPDDR Compression Attached Memory Module	PS-72
	36	APAPG: Address Pre-Processed ALPG for High-Speed Linear Test	PS-73
	52	Detecting and assignment of unexpected tasks in SoC design process using genetic programming	PS-74
	76	Timing Analysis with Analytical Sensitivity	PS-75
	80	Double-Row Flip-flop Design Under Advanced Technology and Its IC-Level Effects	PS-76
	199	Optimized Instruction-set Architecture for Programable Memory Test Pattern Generation	PS-77
	212	Optimized Multiplier Architecture: Integrating Det/Pre-Encoder and Compound gate	PS-78
	216	LIBMixer: An all-MLP Architecture for Cell Library Characterization and DTCO	PS-79
	217	Production-Oriented Design for High Parallel Test Efficiency	PS-80
	221	FedEDA: Federated Learning Framework for Privacy-Preserving ML-EDA	PS-81
	222	PC-Opt: Partition and Conquest-based Optimizer using Multi-Agents for Complex Analog Circuits	PS-82
	225	VeriLogos: Automatic Verilog RTL Generation using Large Language Models	PS-83
	229	Architecture Design Based on MGO (Memory Grid Occupancy) and Data Reuse for Pedestrian Detection	PS-84
	234	RL-Fill: Timing-Aware Fill Insertion Using Reinforcement Learning	PS-85
	246	High Quality Power-Aware Verification of Mixed Signal designs using UPF checkers	PS-86
	254	Device Parameter Extraction Method for Training Performance Predicting Models	PS-87
Wireline	49	A CMOS Fully Differential Transimpedance Amplifier for LiDAR Sensor Applications	PS-88
	58	Design and Evaluation of a Low-Swing Output Driver for High-Speed Interfaces	PS-89
	94	Analysis of Test Environment Configuration for High-Speed Link Chip Measurement	PS-90
	240	A Discrete Multitone Wireline Transceiver With Clipping Ratio Optimization For ADC-Based High-Speed Serial Links	PS-91

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AUGUST 21, 2024 (DAY 2)

* Poster Set-up & Exhibition : August 21, 08:30 ~ 12:00
* Standing Time : August 21, 11:15 ~ 11:55

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	314	Designing a Stopwatch using the 7-Segment	UR-02
	316	Pre-boosting Fine Regulation Digital LDO for High Speed SoC Applications	UR-03
	317	Algorithm of tracking PT-symmetric condition for robust WPT system	UR-04
	318	A Fully Integrated FVF Low-Dropout Regulator Acheving Fast Transient Response for SoC	UR-05
	319	Circuit-level optimization of nonideal Neuromophic system for inference accuracy	UR-06
	321	Systolic array-based AI accelerator - KHUPU design with lightweighting technique	UR-07
	323	Exploring and Improving the Utilization of a Braille Recognition Model with YOLO V7	UR-08
	324	Optimizing 3D Cross Point Arrays with Cell Design Considerations for Enhanced Stability and Efficiency	UR-09
	325	Implementation of Traffic Enforcement Cameras for Right Turn Stop Law	UR-10
	326	Analysis of Resistive Analog In-Memory Computing Architecture	UR-11
	327	Safety Helmet Management System using Classical Methods	UR-12
	328	Smart Wardrobe Coordinator	UR-13
	329	Autonomous Vehicle (1/10 Scale Model)	UR-14
	330	Compulsory Electric Scooter Helmet	UR-15
	331	Object Detecting and Signal Controlling System using Yolov7	UR-16
	332	Efficient Hardware Implementation of Softmax and Sigmoid Functions for Enhancing Transformer Model Performance	UR-17
	333	Noise-Efficient Discrete-Time Low-Noise Amplifier	UR-18
	334	A Low Power Consumption 8.1-9.8 GHz CP-PLL Using a LC VCO	UR-19
	335	Design of Charge Pump for Low Noise Phase-Locked-Loop	UR-20
	336	FPGA-Based Nonlinear Function Acceleration for Enhancing LLM Performance	UR-21
	337	Delay Auto-Calibration for Data Bus in Chip-to-Chip Communication of 3D ICs	UR-22
	338	Area Efficient 12-bit Current DAC	UR-23
	339	YOLOv8 Automatic Weapon Control with Edge-Cloud Integrated Look-Ahead Movement Estimator	UR-24
	340	A Highly Linear Wide Bandwidth Programmable Gain Amplifier in 0.18μm CMOS Process	UR-25
	341	A Fast-Lock Integer-N Multi-Phase PLL	UR-26
	342	Design of Stochastic Computing - based Multiplier Circuit using Low Power and High Performance D Flip-Flop	UR-27
	343	Dynamic Instruction Scheduling with Out-of-Order Processing	UR-28
	344	Perceptron based Hybrid Dynamic Branch Prediction Design	UR-29
	345	Advanced Quantized BNNs for Edge Devices	UR-30
	346	Kernel PCA-Enhanced Transformers for Robust Image Recognition	UR-31