Regular Paper [Poster]

AUGUST 20, 2024 (DAY 1)

* Poster Set-up & Exhibition : August 20, 14:00 ~ 18:00
* Standing Time : August 20, 16:55 ~ 17:45

Track	Paper ID	Title
Analog Circuits	5	A Hierarchical Tree-Structured Control Digital Low Drop-out Regulator with Status-Dumping Mechanism
	26	A bandgap reference with low TC of 1.363ppm/℃ across wide temperature range for PMICs
	28	An Ultra Low Temperature Coefficient Bandgap Voltage Reference with Fully MOS Mirror Mapping Circuitry
	38	An All-Digital Standard-Cell-Based Resistive-Sensing Display Panel/Chip Crack Detector
	54	A Fully Integrated Three Level Voltage Regulator with Fast Load Transient Response Using Current build-up mode in 28nm technology for SoC
	60	3 Level Fully Integrated Voltage Regulator with Package Bond Wire Inductor for IoT Applications
	71	Power-efficiency estimation of exponential horn driver circuit for low-power optical link
	73	Phase Locked Loop with Ramp Generator for FMCW LiDAR TX in 28-nm CMOS
	140	A DLL-Based Three-Step Time-to-Digital Converter for Time-of-Flight Applications
	171	A Resilient All-Digital PLL Using Ping-Pong Delay Line
	184	34.8 dB Gain, 7.7GHz Unity Gain Frequency, 4.2 mW Operational Transconductance Amplifier with Current Re-used Feed-Forward Technique
	189	Low-Power Frequency-Mode Temperature Sensing Circuit with Subthreshold Operational Amplifier
	207	A Low-Dropout Voltage Regulator for High-Input Voltage and Wide-Range Load Current Applications
	211	A highly noise-immune TSP readout system with 2nd-order bandpass filtering current conveyor AFE
	251	Reconfigurable Gaussian filtering TSP readout circuit for Flexible AMOLED Display
Circuits and Systems for Emerging Technologies	16	Signal Shifting-based Reusable Redundant TSV Structure for Infrastructure TSV
	104	3T1R Memristor Crossbar Architecture for Diverse Logic Implementation
	107	An Efficient Error Correction Method for DMFBs with Node Redundancy Considering Node Levels
	208	Calibrating the Dark Count Rate of Single Photon Avalanche Diodes Using Linear Regression
	213	Optimized Stochastic Computing based Median Filter
	247	Modeling of Chiplet-based 2.5D Packaging with Silicon Bridge
Digital Circuits, Architecture, and Systems	7	22/16nm High Speed and Area Efficient Automotive Grade STT-MRAM Memory Compiler for 2~128Mb
	8	Design of Digital Lock-in-Amplifier SoC for Gas Pipeline Inspection
	11	A 28-nm 10.4-fJ/b Cryogenic embedded DRAM with 3T1C Gain Cell and MBIST at 4-Kelvin
	22	Kyberator: A High-Efficiency FPGA-Based Multi-Mode CRYSTALS-Kyber Accelerator for Quantum-Resistant Security Applications
	32	Comparison of the Bitonic Sorter for ORBGRAND
	34	A Resource-Efficient Multi-core Multi-thread RISC-V-based System-on-Chip
	53	A Delay Calibration Circuit for Time-Controlled Pre-Emphasis up to 3.8Gbps in Memory Interfaces
	56	Fast-Lock ZQ Calibration Utilizing Charge Injection Technique for High Density Memory Systems
	63	Effective Data-Width Aware ECC Scheme for HBM
	65	Cost-Efficient Partially-Parallel LDPC Decoder Architecture for 50G-PON Standard
	69	Evaluating the Impact of In-band ECC on GPU Performance
	95	Improved Contrast Enhancement Algorithm for Night Vision Systems using Thermal Camera
	96	Optimizing Transformer Hardware Acceleration: Advancing GELU Activation with Innovative Data Representation Techniques
	105	Low-error Fixed-width Booth Multiplier with High-radix Booth Encoder
	111	FPGA Design of a Masked AES Circuit with PPRM-based S-Box
	116	Enhancing Efficiency in Computational Intensive Domains via Redundant Residue Number Systems
	128	Design of a 3D-IC based AI-Vision SoC
	155	Analysis and Design of CRC-based SENT Interface for Future Automotive Applications
	159	An Approximate Multiplier Design Based on Mitchell's Algorithm
	164	A Two-level Tracking Mechanism to Mitigate RowHammer Attacks
	166	Integration of IP-Cores for the M3 Architecture with Low Area Overhead: Accelerator Support Module
	187	PEMAC: A Posit EMAC with LDD & Logarithm Approximation
	231	On-Device Eye Tracking System with Dual Lightweight AI Processors
	237	The hardware implementation of QARMA-64 with RoCC on FPGA for memory encryption
	242	System-on-Chip iot for Smart Poultry Manufacturing
	245	Efficient Hardware Implementation of Nonlinear Activation Function For Inference Model
	273	A Novel Area Efficient Approximate Stochastic Computing Approach for Edge Devices

AUGUST 21, 2024 (DAY 2)

* Poster Set-up & Exhibition : August 21, 13:10 ~ 17:00
* Standing Time : August 21, 15:55 ~ 16:45

Track	Paper ID	Title
Machine Learning and AI	13	Performance evaluation of cloud database in terms of using tenancy model and in-memory database
	39	ON-CNN: Online Arithmetic based CNN Accelerator
	45	A Fully 4-bit Quantized MobileNet-SSD
	77	BS2: Bit-Serial Architecture Exploiting Weight Bit Sparsity for Efficient Deep Learning Acceleration
	120	Resource-efficient DL Model Inference with Weight Clustering and Zero-skipping
	121	Fast Performance and Power Profiler for SRAM Compute-in-Memory-based Accelerators
	133	Simplified Real-time Categorized Vehicle Counting and Speed Estimation
	135	Error-Resilient Binary Neural Network Inference with Selective Recompute-Based Error Correction
	156	Hardware-aware Hierarchical Transformer using Softmax Low Probability Prediction
	162	Integrating Noise Classification and Speech Enhancement Model for Hearing Aids
	174	Integrating CNN and RCE Networks for Efficient On-Device Image Classification
	194	A Hybrid Precision Network and Binary Processing Elements for 3D Hand Pose Estimation
	220	Strategic Improvements in CNN Accelerators: Optimizing PE Utilization for MobileNetV2
	236	Autoencoder-based Knowledge Distillation For Quantized YOLO Detector
	243	Row-Efficient Pruning for In-Memory Convolutional Weight Mapping
	244	An Im2col Architecture Using The Benes Network For Deep Learning Hardware Accelerators
	250	C-AFA: A Conditionally Approximate Full Adder for Efficient DNN Inference in CIM Arrays
	263	Generative Adversarial Network (GAN)-based Spiking Neural Network Training Methodology to Improve Computing Accuracy
	269	Lightweight DL-based Drone Image Classification for Surveillance Applications
	275	Tailoring Backbone Architectures for SSD
RF/Microwave/Wireless	30	1×8 patch antenna array on glass/PCB substrate
	125	A 60 GHz CMOS OOK Receiver with 7.7 GHz Bandwidth for Wireless Proximity Communication
	142	A 5.8GHz Bootstrap Rectifier for Wireless RF Power Tranfer
	143	Low-cost SDR-based Reader for Chipless Sensor Tag
	198	Differential Injection-Locked Frequency Tripler with a Low-coupling 8-shaped Transformer
SoC Design Methodology and CAD	14	LogicEdu: Enhancing Computational Logic Understanding through Web-Based Boolean Logic Simplification Tool
	21	Scan Architecture with Data Observation for Multiple Scan Cell Fault Diagnosis
	33	INC: In channel Crossing ECC for LPDDR Compression Attached Memory Module
	36	APAPG: Address Pre-Processed ALPG for High-Speed Linear Test
	52	Detecting and assignment of unexpected tasks in SoC design process using genetic programming
	66	Leveraging Assertion-Based Verification for Pipe-lined Architecture Validation
	67	Verification Data Lake for SoC Design Verification
	68	Regression Management with ML and Rule based AI
	76	Timing Analysis with Analytical Sensitivity
	80	Double-Row Flip-flop Design Under Advanced Technology and Its IC-Level Effects
	199	Optimized Instruction-set Architecture for Programable Memory Test Pattern Generation
	212	Optimized Multiplier Architecture: Integrating Det/Pre-Encoder and Compound gate
	216	LIBMixer: An all-MLP Architecture for Cell Library Characterization and DTCO
	217	Production-Oriented Design for High Parallel Test Efficiency
	221	FedEDA: Federated Learning Framework for Privacy-Preserving ML-EDA
	222	PC-Opt: Partition and Conquest-based Optimizer using Multi-Agents for Complex Analog Circuits
	225	VeriLogos: Automatic Verilog RTL Generation using Large Language Models
	229	Architecture Design Based on MGO (Memory Grid Occupancy) and Data Reuse for Pedestrian Detection
	234	RL-Fill: Timing-Aware Fill Insertion Using Reinforcement Learning
	246	High Quality Power-Aware Verification of Mixed Signal designs using UPF checkers
	254	Device Parameter Extraction Method for Training Performance Predicting Models
Wireline	49	A CMOS Fully Differential Transimpedance Amplifier for LiDAR Sensor Applications
	58	Design and Evaluation of a Low-Swing Output Driver for High-Speed Interfaces
	94	Analysis of Test Environment Configuration for High-Speed Link Chip Measurement
	240	A Discrete Multitone Wireline Transceiver With Clipping Ratio Optimization For ADC-Based High-Speed Serial Links

U-REF [Poster]

AUGUST 21, 2024 (DAY 2)

* Poster Set-up & Exhibition : August 21, 08:30 ~ 12:00
* Standing Time : August 21, 11:15 ~ 11:55

Track	Paper ID	Title
Undergraduate Research Exhibition Fair	304	Using electrochemical immunosensor to detecting acute myocardial infarction in ambulance before arriving hospital
	313	A 7.4MHz, 91.5% Efficient Dual Mode Buck Converter for Communication and Wearable Applications
	314	Designing a Stopwatch using the 7-Segment
	315	Design of Ultralow Power Buck Converter using Hysteretic Control Achieving 86.6% Efficiency
	316	Pre-boosting Fine Regulation Digital LDO for High Speed SoC Applications
	317	Algorithm of tracking PT-symmetric condition for robust WPT system
	318	A Fully Integrated FVF Low-Dropout Regulator Acheving Fast Transient Response for SoC
	319	Circuit-level optimization of nonideal Neuromophic system for inference accuracy
	321	Systolic array-based AI accelerator - KHUPU design with lightweighting technique
	322	Design of a Bandgap Reference for a Low-Dropout Regulator with High Conversion Rate
	323	Exploring and Improving the Utilization of a Braille Recognition Model with YOLO V7
	324	Optimizing 3D Cross Point Arrays with Cell Design Considerations for Enhanced Stability and Efficiency
	325	Implementation of Traffic Enforcement Cameras for Right Turn Stop Law
	326	Analysis of Resistive Analog In-Memory Computing Architecture
	327	Safety Helmet Management System using Classical Methods
	328	Smart Wardrobe Coordinator
	329	Autonomous Vehicle (1/10 Scale Model)
	330	Compulsory Electric Scooter Helmet
	331	Object Detecting and Signal Controlling System using Yolov7
	332	Efficient Hardware Implementation of Softmax and Sigmoid Functions for Enhancing Transformer Model Performance
	333	Noise-Efficient Discrete-Time Low-Noise Amplifier
	334	A Low Power Consumption 8.1-9.8 GHz CP-PLL Using a LC VCO
	335	Design of Charge Pump for Low Noise Phase-Locked-Loop
	336	FPGA-Based Nonlinear Function Acceleration for Enhancing LLM Performance
	337	Delay Auto-Calibration for Data Bus in Chip-to-Chip Communication of 3D ICs
	338	Area Efficient 12-bit Current DAC
	339	YOLOv8 Automatic Weapon Control with Edge-Cloud Integrated Look-Ahead Movement Estimator
	340	A Highly Linear Wide Bandwidth Programmable Gain Amplifier in 0.18μm CMOS Process